This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**

THIS PAGE BLANK (USPTO)

GB 2247779 (1)
H01L27/02B4F-

- 1- *- H01L27/02B4F

THE PATENTS ACT 1977

SPECIFICATION NO. 2 247779A
The following corrections were allowed under Section 117 on 13 April 1992

Heading (72)

after Yun -Seung delete Sin insert Shin

before Kang delete Jun insert Jon

THE PATENT OFFICE

26 May 1992

2247779

SEMICONDUCTOR DEVICE

The present invention relates to a semiconductor device, and particularly to a highly reliable semiconductor device which is tolerant of electrostatic discharge.

Generally, a CMOS integrated circuit has several advantages, e.g., high noise resistance and low power consumption. Accordingly, the design tendency of DRAM devices has been converted from a NMOS type to the CMOS type with the advancement of higher packing density and miniaturizing techniques. At the same time, it has continuously proceeded to prevent the device from the deterioration of characteristics due to the latchup phenomenon and the electrostatic damage, which are inherent problems of the CMOS circuit. In particular, the electrostatic damage (ESD), which is caused by the discharge of triboelectricity produced between two materials such as plastics or between human body and clothing, can destroy the CMOS integrated circuit to lower the reliability of the device. It is known that the primary cause of the electrostatic breakdown is a puncture phenomenon of a gate oxide layer by the static electricity applied to an input terminal. The breakdown of the gate oxide layer has been conventionally prevented by adopting a protective circuit including a resistor, diode, and the like in a gate input stage. The secondary cause of the electrostatic breakdown is known to be a junction breakdown of the elements of an output stage by the static electricity which is applied to an output terminal.

The junction breakdown of the elements of the output stage by the static electricity will be explained in detail with reference to Figure 1 of the accompanying drawings. In a conventional ESD tolerance testing of Figure 1, an ESD test device 2 is connected between an output terminal OT and a ground terminal Vss of a chip 1. The ESD test device 2 can be expressed by an equivalent series circuit including a switch SW, a resistor RT and a capacitor CT. The ESD test is performed as follows. At first, the capacitor CT is charged by hundreds to thousands of volts. Then, the switch SW is turned on, the static electricity charged in the capacitor CT is thus discharged through the chip 1 and, the degree of the resultant damage in the chip is checked. The discharging current Io of the test will flow through pull-down transistor M2 of the output stage to be grounded.

In Figure 2 of the accompanying drawings, when the charged voltage of the capacitor CT is positive, a n+p drain junction 15a of the pull-down transistor M2 will be reversely biased and n+p source junction 15b of the transistor M2 will be forward biased, so that the breakdown occurs in the n+p drain junction 15a by the high voltage applied to a drain metal wiring layer 16b and, simultaneously, the discharging current Io is to flow from the drain junction 15a toward the source junction 15b. Under the condition that the switch SW is turned off, the electrostatic energy E stored in the capacitor CT with 100pF can be obtained by the following equations, when the voltage charging to the capacitor CT is 2000V.

$$E = \frac{1}{2} CV^2$$

$$= \frac{1}{2} (100pF) \times (2000V)^2 = 0.2\ mJ$$

That is, charged energy of 0.2mJ stored in the capacitor CT is dissipated through the resistor RT of the ESD test device 2 and the pull-down transistor M2 of the output stage of the chip 1. Here, if the resistance of the element of the output stage is small, the discharging time constant τ is written as:

$$\tau \fallingdotseq RT \cdot CT = 100pF \times 1.5K\Omega$$
$$= 0.15\mu\ sec$$

where the resistance RT of the resistor is 1.5KΩ. Therefore, the mean power dissipation W is as follows:

$$W = \frac{E}{\tau} = \frac{0.2mJ}{0.15\mu\ sec} \fallingdotseq 1.3KW$$

This denotes that the total charged energy of 0.2mJ is dissipated at the power of about 1.3KW through the resistor

RT and the reversely biased n+p drain junction region 15a in the pull-down transistor M2 of the output stage of the chip, for about 0.15μ sec. Therefore, heat which is proportional to the value obtained by multiplying the reversely biased voltage (generally 10 to 30V) by discharging current Io is generated in the junction portion. Due to the heat, the drain metal electrode layer 16b having low melting point is liable to be melted, or the reaction between metal and silicon in the junction may cause short between the drain metal electrode layer 16b and the substrate 10. As a result, the n+p junction 15a is destroyed to increase the leakage current, thereby deteriorating the operation characteristic of the elements. With the adoption of the higher packing density and the miniaturization in the CMOS integrated circuit, the depth of n+ layers 15a and 15b has been shallowed to be roughly 0.2 to 0.7㎛ so as to reduce the short channel phenomenon. If the depth of a junction spiking 18, which occurs in the contact portion of the metal wiring layer 16b and the silicon substrate 10 to extend into the silicon substrate 10, exceeds the depth of the n+ layer, this gives rise to the increase of leakage current and the decrease of the junction breakdown voltage to deteriorate characteristics of the elements, thereby worsening the reliability.

Therefore, in the conventional method, a resistor was inserted between the output terminal OT and the drain terminal of the pull-down transistor M2 to increase the discharge time constant τ so as to reduce the peak current or dissipate the energy consumption. But, in this case, the variation of the output voltage is repressed by lowered output current caused by the inserted resistor, thus results in lowering the operation speed. Accordingly, the n+ junction layer having a resistance of about 10Ω and below, or a low resistance wiring layer such as doped polycrystalline silicon, or the like, are conventionally utilized. But it does not reveal desirable effects in protecting the output stage from the ESD due to the restrictions such as decrease of operation speed as described above.

Alternatively, it is reported that the melting reaction between the silicon substrate and the metal layer is prevented by interposing a metal layer formed by refractory metal such as W, Mo, Ti, Ta or Co on the contact portion, thereby improving the tolerance of the contact portion to the ESD. But, the ESD tolerance of the junction in the transistor of output stage is not directly increased by this method.

Therefore, it is an object of the present invention to provide a highly reliable semiconductor device having contact junction structure tolerant of ESD in order to solve the above described problems of the conventional techniques.

To achieve these and other objects, the device according to the present invention comprises:

a semiconductor substrate of a first conductive type;

a shallow junction region of a second conductive type formed in the substrate with a predetermined depth from the surface of the substrate;

a low resistant wiring layer formed on the substrate by interposing an insulating layer, and contacting the shallow junction region through contact holes formed on the insulating layer to be connected to an output terminal; and

a deep junction region of the second conductive type which is formed in the substrate, includes a contact region in the shallow junction region, and has a depth for sufficiently surrounding a junction breakdown portion generated at the contact region of the low resistant wiring layer and the shallow junction region and extending into the substrate by static electricity fed to the output terminal.

Here, the shallow junction region is a drain or a source region of the transistor of the output stage.

The CMOS semiconductor device including the device of the present invention is preferably formed in such a manner that a conventional MOS transistor having only a shallow junction region is interposed between a MOS transistor having a second conductive type deep junction region and a conventional MOS transistor formed in the second conductive type well region, consequently, the problems such as latchup phenomenon can be effectively prevented.

The CMOS semiconductor device having the aforementioned structure of the present invention, is preferably manufactured in such a manner that the deep junction region is simultaneously formed with the formation of the second conductive type well of a CMOS semiconductor device. Thus, according to the method of the present invention, the semiconductor device can be simply manufactured by only changing the layout design without any additional manufacturing process.

Embodiments of the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is an equivalent circuit diagram illustrating an ESD test of an output stage of a conventional CMOS integrated circuit;

Figure 2 is a sectional view showing the structure of an output stage element of a conventional CMOS integrated circuit;

Figure 3 is a sectional view showing the structure of a semiconductor device according to an embodiment of the present invention; and

Figures 4A to 4K are process diagrams successively showing processes for manufacturing an embodiment of the CMOS semiconductor device of the present invention.

In the highly reliable semiconductor element shown in Figure 3, second conductive type shallow junction regions 22a and 22b formed to a depth of 0.2~0.7㎛ in a first conductive type semiconductor substrate 20 contact low resistant wiring layers 24a and

24b formed on the semiconductor substrate 20 through contact holes 25a and 25b formed in an insulating layer 28. The semiconductor element includes the contact portion in the shallow junction regions 22a and 22b and second conductive type deep junctions 26a and 26b having a depth of 3~ 6㎛ formed in the semiconductor substrate 20. The depths of the deep junction regions 26a and 26b are respectively determined to sufficiently surround a junction spiking 29 produced by electrostatic discharge in the contact portion of the low resistant wiring layers 24a and 24b and the shallow junction regions 22a and 22b. Here, if the element is NMOS transistor, the first conductive type is of p-type impurity and the second conductive type is of n-type impurity. When it is PMOS transistor, the first conductive type is of n-type impurity and the second conductive type is of p-type. The reference numeral 23 denotes a gate electrode layer and 27 denotes a field oxide layer. Thus, even though the junction spiking 29 occurs in the contact portion 25b by the static electricity, the spiking 29, i.e., junction breakdown portion can not have influence on the first conductive type semiconductor substrate 20 due to the deep junction region 26b, in the aforesaid highly reliable semiconductor element.

Here, forming the deep junction region under the contact region can be performed in such a manner that the n+ or p+ deep junction region is formed within the shallow junction region by implanting a phosphorus or a boron ion only into the contact region by using the thick insulating layer 28 formed around the contact holes as a mask, after forming the contact holes 25a and 25b. However, this requires additional ion implantation process and two photolithography processes so as to separately implant n+ or p+ impurities. Moreover, as the element already formed with the contact region cannot endure the high-temperature annealing process, the activation of the P+ and B+ ions implanted into the contact region cannot easily be achieved.

Therefore, a method for manufacturing the highly reliable CMOS semiconductor device of the present invention adopts the processes illustrated in Figures 4A to 4K, wherein, when the formation of the second conductive type well is performed as in the conventional CMOS semiconductor manufacturing process, the deep junction region is simultaneously formed under the contact region, so that the above described drawbacks of the conventional manufacturing method is complemented and the ESD tolerance of transistor of the output stage can be enhanced.

The process shown in Figures 4A to 4K is of the case wherein a double-well CMOS process for the p-type substrate and n+ doped polycrystalline silicon gate are utilized.

Referring to Figure 4A, a pad oxide layer 101 having a thickness of about 300Å is thermally grown in oxide atmosphere at 1000℃ on a 100 crystal oriented p-type silicon substrate 100 with a relative resistance of about

10Ω -cm . A nitride layer 102 made of Si_3N_4 having a thickness of about 100Å is deposited via a Chemical Vapor Deposition method on the pad oxide layer 101. Thereafter, the nitride layer 102 formed on n-well regions 104a, 104b and 105 shown in Figure 4C which will be described later is removed by conventional photoetching method, and phosphorus ion (P+) is implanted with a dose of 10^{13} /cm² and at the energy of 100KeV by using the residual nitride layer 102 as a mask.

Referring to Figure 4B, an oxide layer 106 having a thickness of about 4000Å is thermally grown by using the resultant nitride layer 102 as a mask, and the residual nitride layer 102 is then removed. Thereafter, boron ion (B+) is implanted with a dose of 3×10^{12} /cm² and at the energy of 30KeV by using the oxide layer 101 as a mask in order to form a p-well 108 illustrated in Figure 4C which will be described later.

Referring to Figure 4C, after the phosphorus ion (P+) and boron ion (B+) are implanted, the semiconductor substrate 100 is driven-in for about 12hours at a temperature of about 1,150℃, and then, the implanted ions are thermally diffused and the n-wells 104a, 104b and 105 and p-well 108 of a depth of about 4㎛ are formed. The oxide layers 101 and 106 on the semiconductor substrate are then removed , and a SiO_2 layer 110 having a thickness of about 200Å is grown by thermal oxidation.

Referring to Figure 4D, a nitride layer 112 made of Si_3N_4 having a thickness of about 1500Å is deposited through CVD on the SiO_2 layer 110 and, then, the nitride layer is removed by photoetching other than the nitride layer 112 on active regions T_1, T_2 and T_3 for forming transistors.

Referring to Figure 4E, the n-well region 105 is covered by a photoresist 116 around the active regions T_1 and T_2 and boron ion (B+) is implanted with a dose of $110^{13}/\mathrm{cm}^2$ and at the energy of about 30KeV in order to form a p-type channel stop layer 114 shown in Figure 4G which will be described later.

Referring to Figure 4F, the photoresist 116 is removed, the region other than the n-well region 105 is then covered by photoresist 120, and phosphorus ion (P+) is implanted in the portion around the active region T_3 with a dose of $10^{13}/\mathrm{cm}^2$ and at the energy of about 100KeV in order to form the stop layer 118 shown in Figure 4G which will be described later.

Referring to Figure 4G, the photoresist 120 is removed, and a field oxide layer 122 having a thickness of about 5000Å is thermally grown in the oxide atmosphere at about 1000℃ by using the residual nitride layer 112 as a mask. Then, the resultant nitride layer 112 is removed by a wet etching process.

Referring to Figure 4H, after the nitride layer 112 is removed, SiO_2 layer 110 is removed and gate insulating layer 124 of each transistor is grown to have a thickness of about 200Å in the oxide atmosphere at 900℃ and, thereafter, a polycrystalline silicon is deposited and patterned through photoetching to form a gate electrode layer 126. Here, in order to reduce the resistance of the gate electrode layer 126, the polycrystalline silicon is doped with n-type impurity by diffusing $POCl_3$ at the temperature of about 900℃ after the polycrystalline silicon is deposited, a refractory or high melting point metal layer and metal silicide layer are then stacked by CVD over the structure obtained by the above, and, thereafter, the gate patterning process can be alternatively performed. Here, any one of tungsten (W), molybdenum (Mo), titanium (Ti), tantalum (Ta) and cobalt (Co) can be used as the refractory metal.

Referring to Figure 4I, after the gate electrode layer 126 is formed, the n-well region 105 is covered by photoresist 128, and an arsenic ion (As+) is implanted with a dose of 5×10^{15}/㎠ and at the energy of 50KeV so as to form drain or source layers 130 of n-channel transistor in the active regions T_1 and T_2.

Referring to Figure 4J, after the photoresist 128 is removed, the region is covered by photoresist 132 other than the n-well region 105, BF_2 + is then implanted with a dose of 5×10^{15}/㎠ and at the energy of 50KeV in order to form drain or source layers 134 of p-channel transistor in the active region T_3.

Referring to Figure 4K, after performing the foregoing ion-implantation process of the drain or source layers, the photoresist 132 is removed, then, a BPSG (Boro-Phosphorus-Silicate Glass) layer 136 is deposited, and a contact hole 138 is formed, and thereafter, low resistant wiring layer 140 is deposited and patterned by a photoetching method, thereby completing the manufacture of the semiconductor element.

Here, aluminum (Al) containing 1% of Si and 0.5% of Cu can be used for the low resistant wiring layer 140, in case that the circuit wiring is formed by depositing the doped polycrystalline silicon and successively depositing the metal wiring layer on the polycrystalline silicon. Especially, in order to solve the problem like short caused by Si precipitation in the contact region with increasing the packing density, the refractory metal layer such as titanium (Ti), nitride titanium (TiN), tungsten (W), molybdenum (Mo), tantalum (Ta) and cobalt (Co) can be sandwiched in the contact region between the aluminum layer and silicon substrate with increasing the packing density. In this way, the ESD tolerance can be enhanced by interposing the refractory metal layer on the contact portion.

As described above, when the deep junction region of the present invention is simultaneously formed with the well during the CMOS manufacturing process, the impurity of the deep junction region is driven-in during the initial stage of the process as compared with the ion implantation performed through contact hole, so that the troublesome in the process for diffusing the impurity in the deep junction region can be eliminated, thus, the highly reliable element of the present invention can be manufactured with much more effective and simpler manner.

In the above descriptions, the device having the n-type deep junction region in the p-type substrate is taken as an example, however, alternatively, such a device that has the p-type deep junction region in the n-type substrate can be manufactured by the same method.

Moreover, the deep n-well junction regions 26a and 26b are formed in both the source and the drain 22a and 22b of the transistor in Figure 3, however, only one out of the source and drain can be formed in case that the junction requiring the ESD tolerance is restricted to only one of the source or drain of the transistor.

CLAIMS

1. A semiconductor device comprising:

a semiconductor substrate of a first conductive type;

a shallow junction region of a second conductive type formed in said substrate with a predetermined depth from the surface of said substrate;

a low resistant wiring layer formed above said semiconductor substrate by interposing an insulating layer, and contacting said shallow junction region through contact holes formed in said insulating layer to be connected to an output terminal; and

a deep junction region of said second conductive type which is formed in said semiconductor substrate, includes a contact region in said shallow junction region, and has a depth for sufficiently surrounding a junction breakdown portion generated at said contact region of said low resistant wiring layer and said shallow junction region and extending into said substrate by static electricity fed to said output terminal.

2. A semiconductor device as claimed in claim 1, wherein said shallow junction region is a source of a MOS transistor.

3. A semiconductor device as claimed in claim 1, wherein said shallow junction region is a drain layer of a MOS transistor.

4. A semiconductor device as claimed in any preceding claim, wherein said low resistant wiring layer is mainly of

aluminium and contains silicon.

5. A semiconductor device as claimed in any preceding claim, wherein said low resistant wiring layer is mainly of aluminum and contains silicon and copper.

6. A semiconductor device as claimed in any of claims 1 to 3, wherein said low resistant wiring layer is made of densely-doped polycrystalline silicon.

7. A highly reliable semiconductor device as claimed in any of claims 1 to 3, wherein said low resistant wiring layer consists of a composite layer of densely-doped polycrystalline silicon, and refractory metal silicide.

8. A semiconductor device as claimed in claim 1, wherein said low resistant wiring layer consists of refractory metal layer.

9. A semiconductor device as claimed in any of claims 1 to 3, wherein said low resistant wiring layer consists of a refractory metal silicide layer.

10. A semiconductor device as claimed in any one of claims 6 to 9, wherein said refractory metal is any one selected from group consisting of tungsten (W), titanium (Ti), tantalum (Ta), molybdenum (Mo) and cobalt (Co).

11. A semiconductor device as claimed in any preceding

claim, wherein said deep junction regi formed with the formation of a well of device.

12. A semiconductor device as clai claim, wherein said semiconductor substra deep junction region is n-type.

13. A semiconductor device as clair 1 to 11, wherein said semiconductor subs said deep junction region is p-type.

14. A semiconductor device comprisi

a first MOS transistor having a f channel in a second conductive type well conductive type semiconductor substrate;

a second MOS transistor having type channel and formed in said semiconduc

a third MOS transistor having a type channel and formed between said first said second MOS transistor in said semicon

said second MOS transistor has a d of said second conductive type which i semiconductor/substrate, includes a contact and a drain region of said second MOS tra depth to sufficiently surround the junction generated at the contact region of said s extending into said semiconductor subs electricity.

claim, wherein said deep junction reg
formed with the formation of a well of
device.

12. A semiconductor device as cla
claim, wherein said semiconductor subst
deep junction region is n-type.

13. A semiconductor device as cl
1 to 11, wherein said semiconductor s
said deep junction region is p-type.

14. A semiconductor device compr
a first MOS transistor havin
channel in a second conductive type
conductive type semiconductor substra
a second MOS transistor ha
type channel and formed in said semic
a third MOS transistor ha
type channel and formed between said
said second MOS transistor in said s
said second MOS transistor
of said second conductive type w
semiconductor/substrate, includes a
and a drain region of said second
depth to sufficiently surround the j
generated at the contact region of
extending into said semiconduct
electricity.

FIG.1 (PRIOR ART)

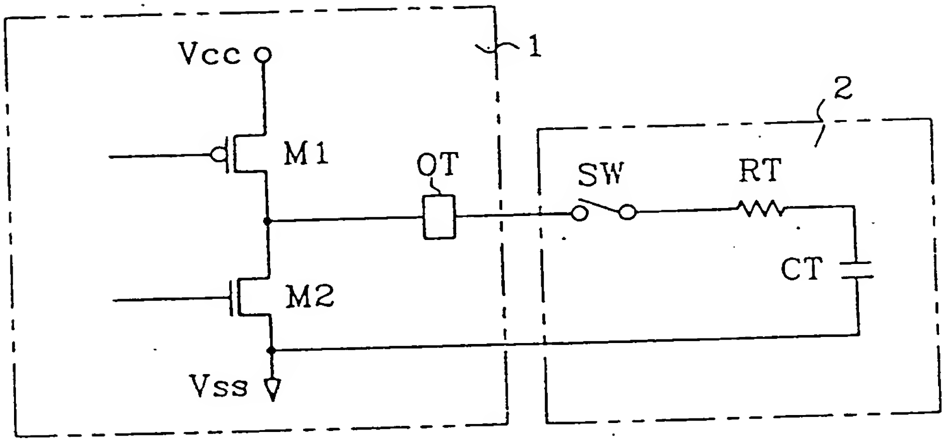
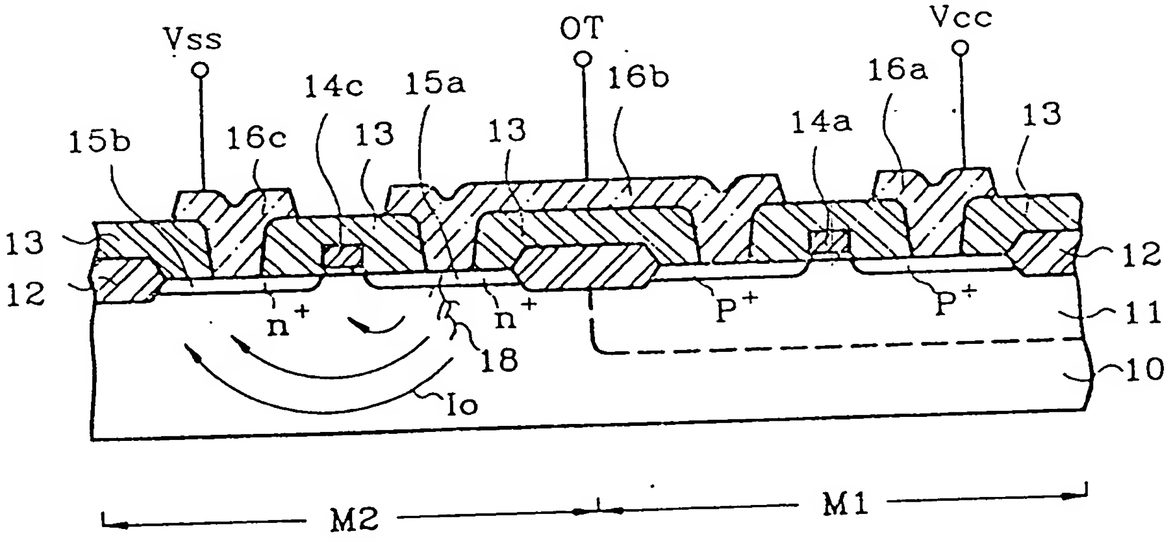

Vcc
1
2
M1
OT
SW
RT
CT
M2
Vss

FIG.2 (PRIOR ART)


Vss
OT
Vcc
16b
16a
14c
15a
15b
16c
13
13
13
14a
13
13
12
12
n+
n+
P+
P+
11
18
10
Io
M2
M1

THIS PAGE BLANK (USPTO)

FIG.4A

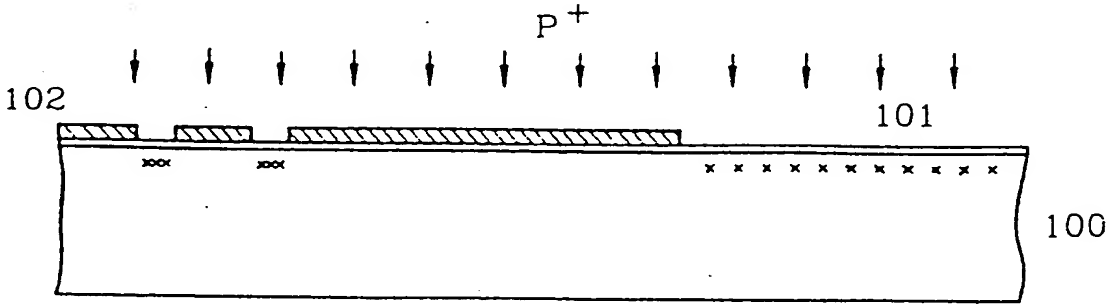

P+
102
101
100

FIG.4B

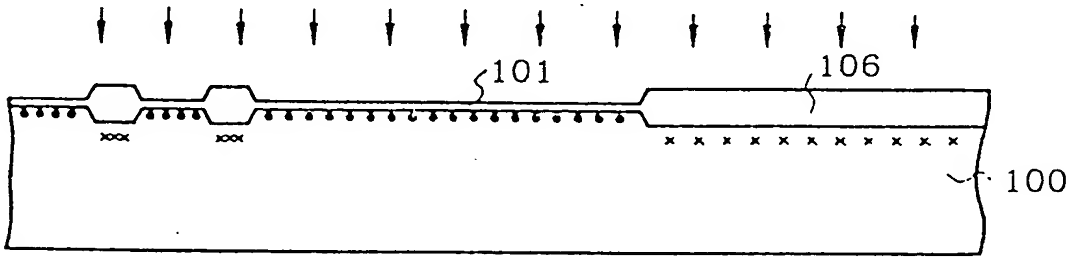


FIG.4C

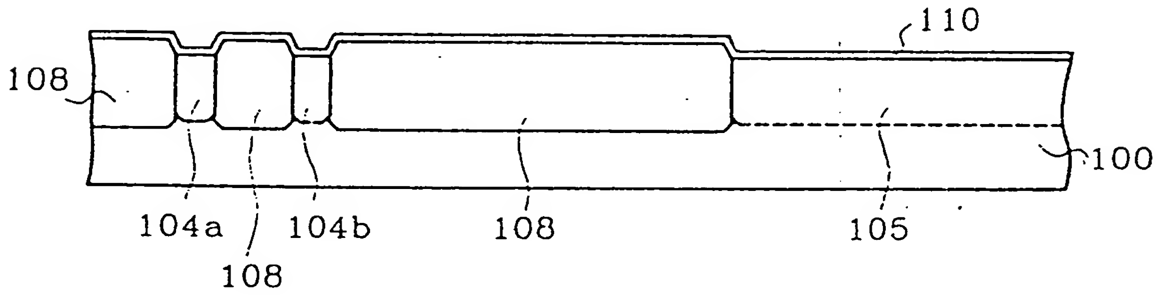
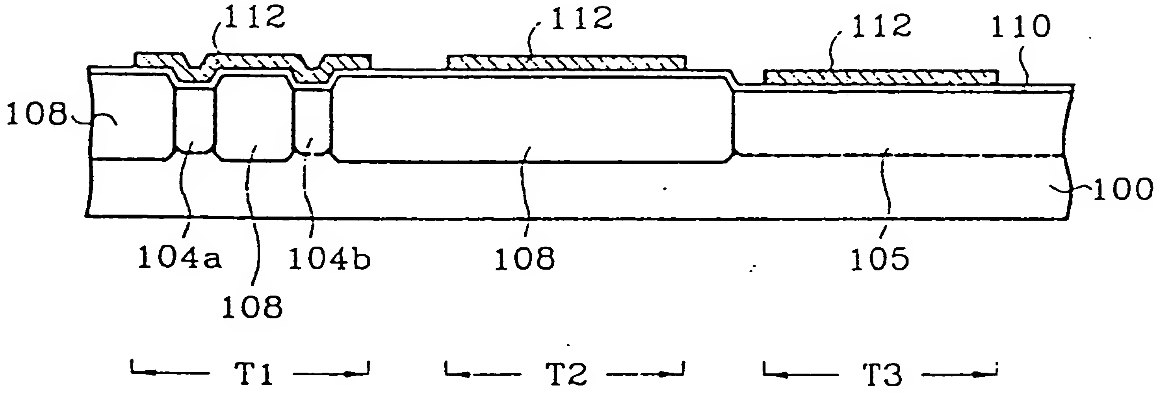

110
108
100
104a
104b
108
105
108

FIG.4D


112
112
112
110
108
100
104a
104b
108
105
108
T1
T2
T3

THIS PAGE BLANK (USPTO)

FIG.4I

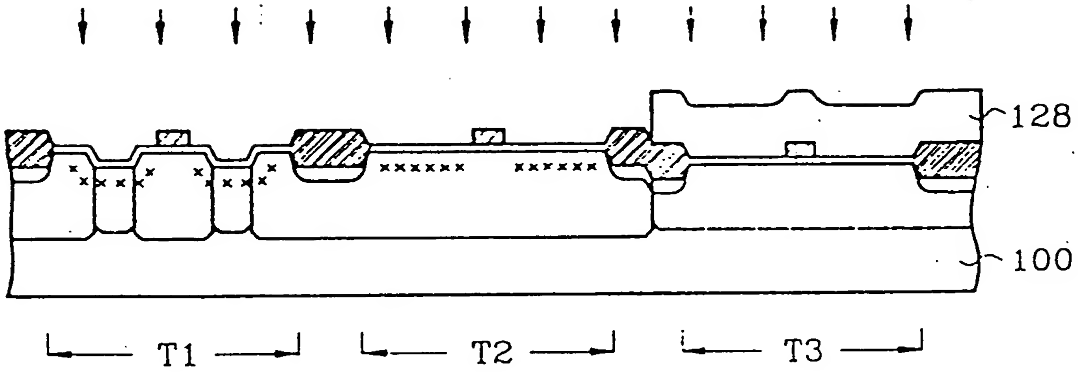

128
100
T1
T2
T3

FIG.4J

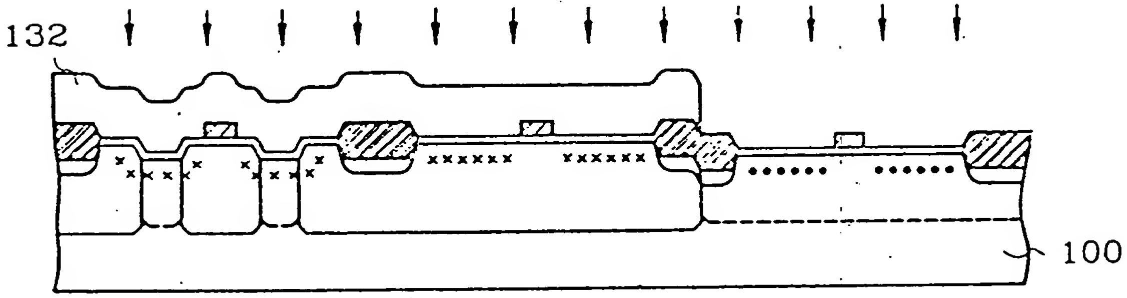
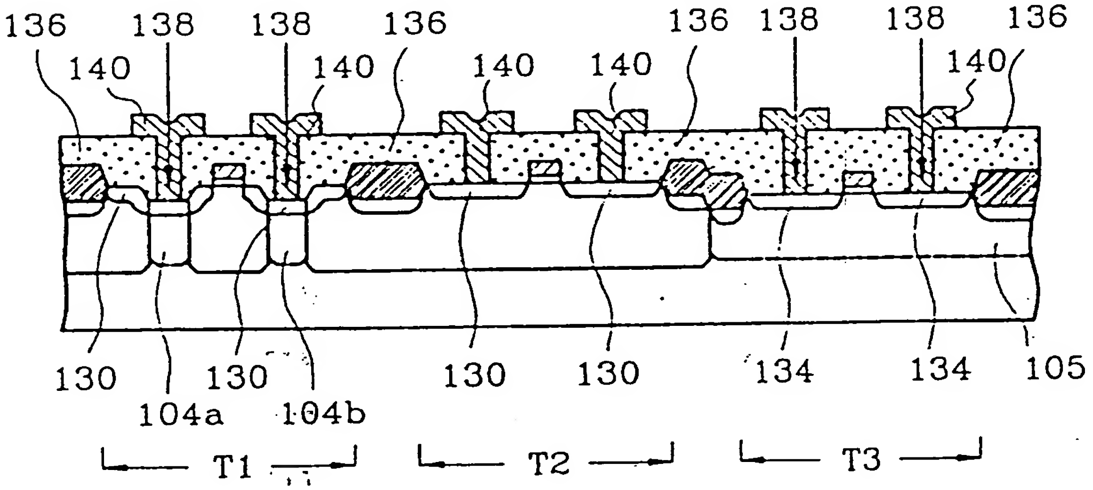


FIG.4K


136
138
138
136
136
138
138
136
140
140
140
140
140
130
104a
130
104b
130
130
134
134
105
T1
T2
T3